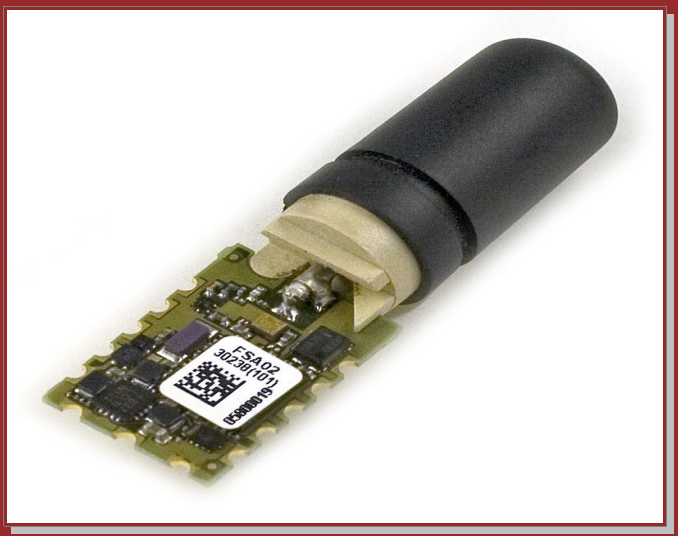
FALCOM
WIRELESS COMMUNICATIONS GMBH

Smart Antenna

FSA02

Application Notes



Version: 1.0.2; Updated: Friday 23 May 2008

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Version history:

This table provides a summary of the document revisions.

Number	Author	Changes	Change date
1.0.0	F. Beqiri	Initial version	18/02/2008
1.0.1	F. Beqiri	Because the FSA02 is based on the JP18 receiver, for more technical specification about it, refer to the manual **"JP18_hardware_manual.pdf"**.	09/05/2008
1.0.2	F. Beqiri	- The firmware version ROM is very early (engineering proof) and was never intended for production use.	23/05/2008

1 INTRODUCTION

This application note comprises a brief description of the operation of the FALCOM Smart Antenna FSA02, the Pad-Design and an application circuit.

1.1 General

The Smart Antenna can operate either from internal ROM or internal FLASH.

Important: *The firmware version ROM is very early (engineering proof) and was never intended for production use.*

1.2 Technical data (in brief)

- ***ROM:***
  - *Output NMEA messages.*
    - ✔ *Baudrate: 4800 bps,*
    - ✔ *RMC, GGA, GSA - (1 x 1 sec.)*
    - ✔ *GSV - (1 x 5 sec.)*
- ***FLASH:***
  - *Output NMEA messages.*
    - ✔ *Baudrate: 38400 bps,*
    - ✔ *RMC, GGA, GSA, GSV - (1 x 1 sec.)*
- ***BOOTMODE:***
  - *To load a new firmware into the internal FLASH use SiRFflash tool version 3.2 or higher .*

Because the FSA02 is based on the JP18 receiver, for more technical specification about it, refer to the manual ***"JP18_hardware_manual.pdf"****.*

1.3 ROM and Flash Memory Operating Modes

	DATA 0	**DATA 1**
ROM	Open	Open
FLASH	Open	Connect to GND
BOOTMODE	Connect to VIO	Open

Table 1: ROM and Flash Memory Operating Modes

1.4 Signal levels

The names and position of the pads can be seen from the Pad-Design, which is added in chapter 3, "Schematics".

Pin name	Level	Function
RES	1.2 V CMOS	Input
GPIO 0	1.8 V CMOS	Input/Output
ON/OFF*	1.2 V CMOS	Input
TM	1.8 V CMOS	Output
VBATT	1.5 V – 5.5 VDC	Input
GND	0 V	-
VCC	3.0 V – 5.5 VDC	Input
GND	0 V	-
DATA 0	1.8 V CMOS	Input at startup
DATA 1	1.8 V CMOS	Input at startup
VIO	1.8 V CMOS	Output
TX	3.3 V CMOS** (if VCC = 3.3 V)	Output
RX	3.3 V CMOS** (if VCC = 3.3 V)	Input

** For more technical details regarding the ON/OFF pin, please refer to the "JP18_hardware_manual.pdf" manual, chapter **6.2**.*

** * The voltage on both pins depends on the supply voltage (VCC)*

Table 2: Signal levels and their function

2 SECURITY

This chapter contains important information for the safe and reliable use of the GPS receiver. Please read this chapter carefully before starting to use this GPS receiver.

2.1 Electrostatic Discharge (ESD)

The FSA02 Smart Antenna contains class 1 devices. The FSA02 Smart Antenna contains components that can be damaged or destroyed by electrostatic discharge. When handling the module, observe the necessary safety precautions against electrostatic discharge (ESD), in accordance with EN 61340-5-1 and the following. The following Electrostatic Discharge (ESD) precautions are recommended:

- *Protective outer garments.*
- *Handle device in ESD safeguarded work area.*
- *Transport device in ESD shielded containers.*
- *Monitor and test all ESD protection equipment.*
- *Treat the FSA02 Smart Antenna as extremely sensitive to ESD.*

2.2 Moisture Sensitive Level (MSL)

The FSA02 Smart Antenna is classified as a MSL3 device. FSA02 is moisture sensitive and need to be handled within proper MSL 3 guidelines to avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation. That means, after the FSA02 Smart Antenna is removed from the vacuum packaging, it must go through reflow for main board assembly within 168 hours (1 week). If this conditions is not met, the module should be baked for 24 hours at 125°C before board mounting.

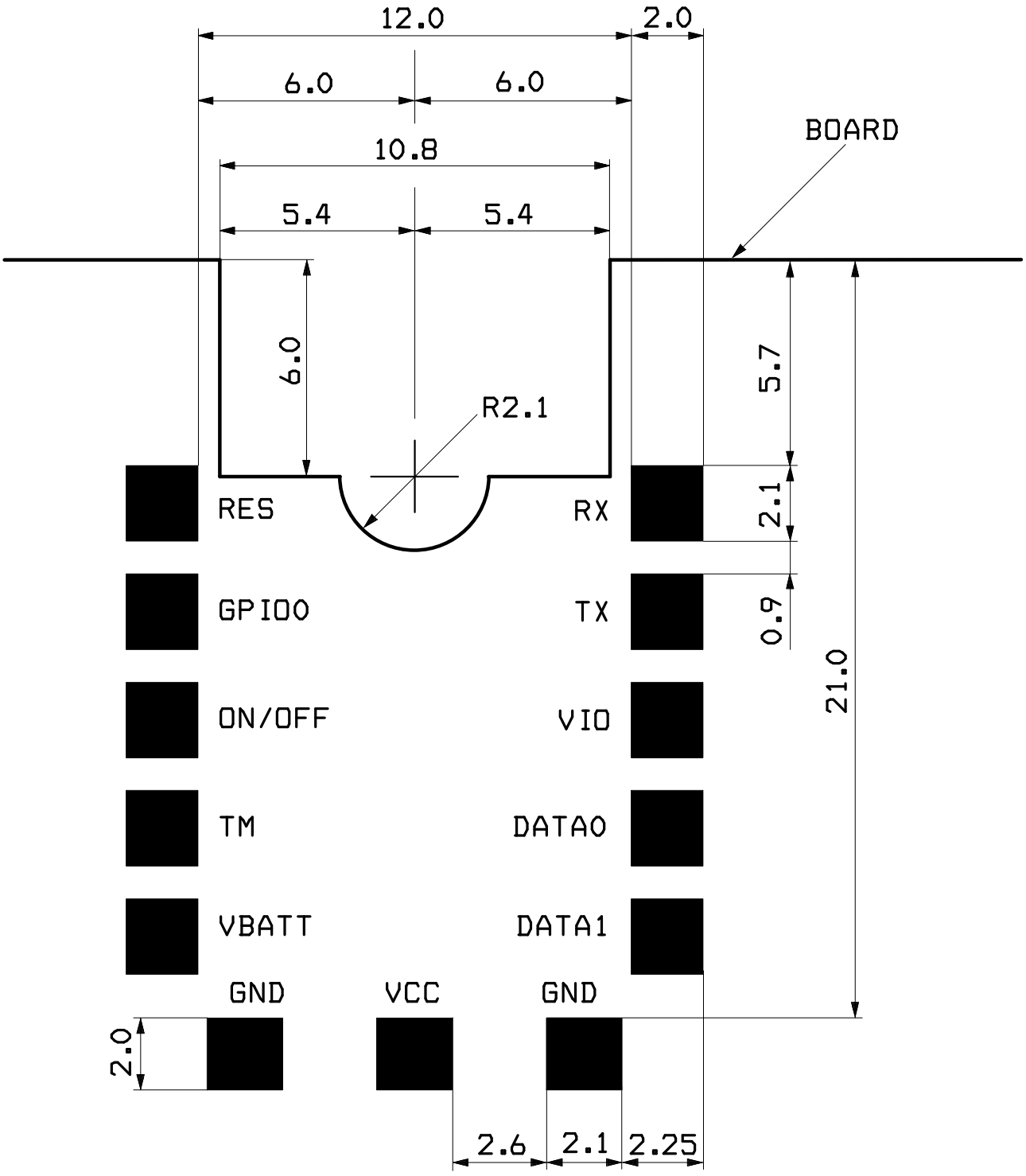
References

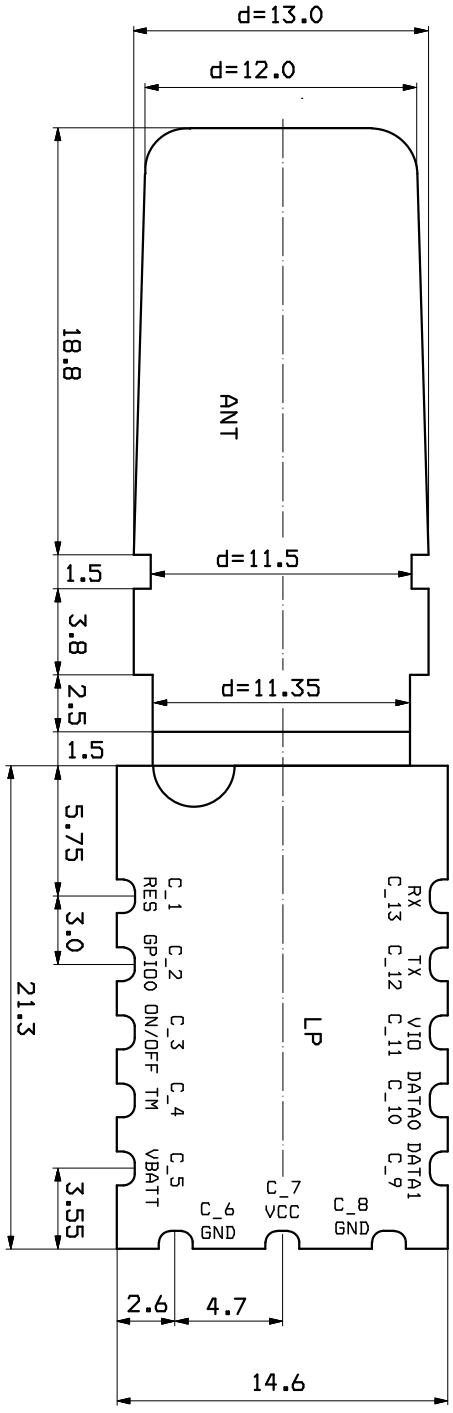
Customers may refer to following IPC standards for more details:

- *J-STD-033B Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.*
- *J-STD-020D Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.*

Pad-design FSA02

Note: no ground under the component

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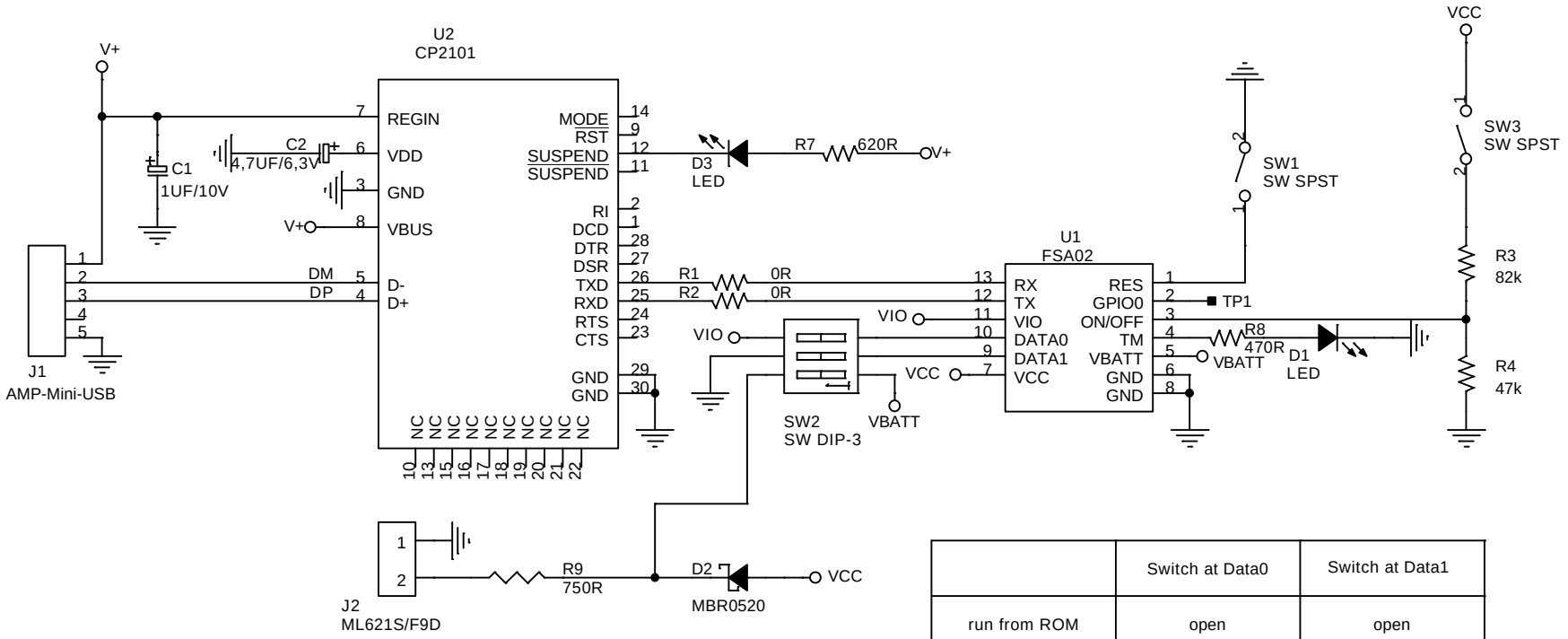
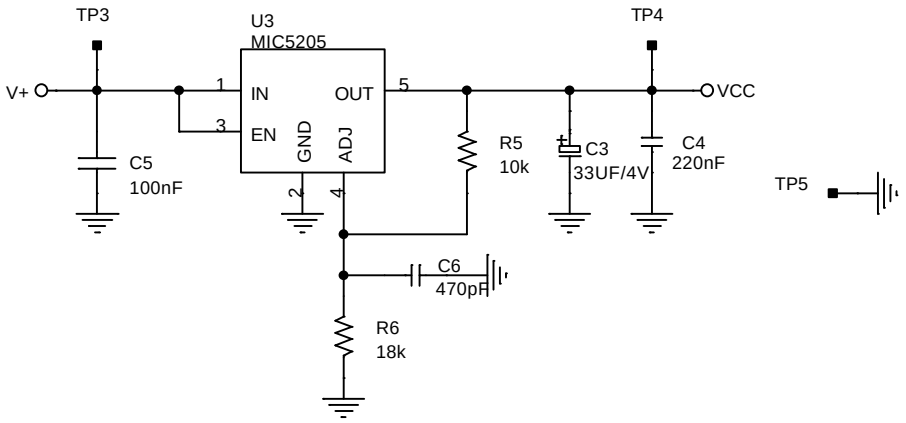
d=12.0
18.8
ANT
1.5
d=11.5
3.8
2.5
d=11.35
1.5
5.75
3.0
21.3
3.55
C_1
RES
C_2
GPIO0
C_3
ON/OFF
C_4
TM
C_5
VBATT
C_6
GND
C_7
VCC
C_8
GND
C_13
RX
C_12
TX
C_11
VIO
C_10
DATA0
C_9
DATA1
LP
2.6
4.7
14.6



	Switch at Data0	Switch at Data1
run from ROM	open	open
run from Flash	open	connect to GND
Bootmode	connect to VIO	open



Note: The dimensions of R3/R4 are for VCC=3.3V

ON/OFF-Level is 1.2V!

Justiermarken

JUST1

JUST2

TP_N1

FALCOM Gewerbering 6 98704 Langewiesen		
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